



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,567	07/24/2003	Jun Funakoshi	108066-00091	1074
4372	7590	10/12/2007	EXAMINER	
ARENT FOX LLP			TRAN, NHAN T	
1050 CONNECTICUT AVENUE, N.W.				
SUITE 400				
WASHINGTON, DC 20036				
			ART UNIT	PAPER NUMBER
			2622	
			NOTIFICATION DATE	DELIVERY MODE
			10/12/2007	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

DCIPDocket@arentfox.com  
IPMatters@arentfox.com  
Patent\_Mail@arentfox.com

<b>Office Action Summary</b>	Application No. 10/625,567	Applicant(s) FUNAKOSHI ET AL.	
	Examiner Nhan T. Tran	Art Unit 2622	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 20 July 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 2-12, 14 and 15 is/are pending in the application.
- 4a) Of the above claim(s) 3-6, 12 and 14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2, 7-11, 15 and 16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 2, 7-11, 15-16 have been considered but are moot in view of the new ground of rejection.

Upon further consideration, the allowable subject matter previously indicated in claim 7 (now recited in claims 7 and 9) has been withdrawn in view of broadest reasonable interpretation of the cited references as set forth below.

The Examiner regrets for any inconvenience caused by this withdrawal of the allowable subject matter.

### ***Claim Objections***

2. Claims 3-6 are objected to because of these claims depend from the canceled claim 1. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2, 7, 8 and 16/2 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 7 recites the limitation "**the result**" in line 6 of this claim. There is insufficient antecedent basis for this limitation in the claim.

Regarding claims 2, 8 and 16/2 are also rejected as being dependent from or incorporated with claim 7.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 9 & 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Koren et al. (US 6,831,686 B1).

Regarding claim 9, Koren discloses an image processing circuit (Figs. 1 & 2), comprising: a correction circuit (Figs. 1 & 2) for adding or subtracting (at summer S1, multiplier S2 and summer S2) an offset (combined values of all  $\alpha(i)$ ,  $1/\beta(i,j)$  and dark  $(i,j,Tint)$  as shown in Figs. 1 & 2 since "*an offset*" is not specifically defined in this claim, thus "*an offset*" is considered as the combined correction values added to or substrated from the image signal to improve image signal quality after CDS and ADC processing as disclosed by Koren) for each column, which is set according to a plurality of columns

Art Unit: 2622

(a plurality of columns of image sensor shown in Fig. 3), to or from pixel signals obtained for each column by amplifying photoelectric conversion signals of pixels, said pixels having photoelectric conversion elements and being arranged in column and row directions (see col. 3, line 4 – col. 4, line 67), wherein said correction circuit further comprises an offset generation section (the whole circuit in Figs. 1 & 2) which compares the pixel signals for each column with a reference value corresponding to brightness of at least one frame of an image (i.e., a reference value of a white sheet of paper), and generates said offset for each column dynamically according to the result of the comparison (col. 3, line 36 – col. 4, line 67, wherein the offset value represented by combined  $\alpha(i)$ ,  $1/\beta(i,j)$  and  $\text{dark}(i,j,T_{\text{int}})$  is generated dynamically based on the output of the pixels and the reference value of the white sheet of paper captured by the image sensor).

Regarding claim 15, Koren also discloses that the reference value is determined based on a gain of an amplifier for amplifying said image signals corresponding to at least one frame of an image (see col. 3, line 61 – col. 4, line 67).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 7, 8, 10, 16/9, 16/10 & 16/15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koren et al. (US 6,831,686 B1) in view of Park (US 2003/0202111 A1).

Regarding claim 7, Koren discloses an image processing circuit (Figs. 1 & 2), comprising:

a sensitivity correction circuit (Figs. 1 & 2) which adds or subtracts (at summer S1, multiplier S2 and summer S2) a predetermined offset (combined values of all  $\alpha(i)$ ,  $1/\beta(i,j)$  and dark  $(i,j,Tint)$  as shown in Figs. 1 & 2 since *"an offset" is not specifically defined in this claim*, thus "an offset" is considered as the combined correction values added to or substrated from the image signal to improve image signal quality after CDS and ADC processing as disclosed by Koren) to or from a pixel signal obtained, for each column, by amplifying photoelectric conversion signals of pixels, and multiplies [the] result by a predetermined gain ( $1/\beta(i,j)$ ), said pixels having a photoelectric conversion element (photodiode) respectively and being arranged in column and row directions (Fig. 3), wherein said predetermined offset includes an offset (combined values of all  $\alpha(i)$ ,  $1/\beta(i,j)$  and dark  $(i,j,Tint)$  as shown in Figs. 1 & 2) which is set according to a plurality of columns (see col. 3, line 4 – col. 4, line 67),

wherein said color sensitivity correction circuit comprises an offset generation section (the whole circuit in Figs. 1 & 2), which compares pixel signals for each column with a reference value corresponding to brightness of at least one frame of an image (i.e., a reference value of a white sheet of paper), and dynamically generates the

second offset according to the result of the comparison (see col. 3, line 61 – col. 4, line 67, wherein the offset value represented by combined  $\alpha(i)$ ,  $1/\beta(i,j)$  and  $\text{dark}(i,j,Tint)$  is generated dynamically based on the output of the pixels and the reference value of the white sheet of paper captured by the image sensor).

Koren teaches a sensitivity correction circuit for an imaging apparatus as discussed above but Koren does not explicitly teach that the sensitivity correction circuit is a **color** sensitivity correction circuit and the predetermined offset includes a first offset which is set according to each **color**.

However, as taught by Park, a color sensitivity correction circuit is disclosed, wherein an offset is set according to each color (e.g., Red offset, Green offset, Blue offset shown in Fig. 6) so that image quality is improved with proper luminance (see Park, paragraphs [0029]-[0030] and [0004]).

Therefore, it would have been obvious to one of ordinary skill in the art to modify the image processing circuit in Koren in view of teaching of Park for correcting color sensitivity by setting an offset to the circuit according to each color so as to improve image quality with proper luminance as suggested by Park.

Regarding claim 8, this claim is also met by the analysis of claim 15

Regarding claim 10, Koren in view of Park also discloses all limitations of claim 10 as analyzed in claim 7 and Fig. 6 of Park, wherein each color is multiplied by a gain value.

Regarding claims 16/9, 16/10 & 16/15, Koren in view of Park discloses a **color** image sensor and the image processing circuit as analyzed in claim 7. Additionally, the combination of Koren and Park also discloses a pixel array where said pixels are arranged in column and row directions (see Fig. 3 in Koren and Fig. 1 in Park); and a column output circuit which is disposed for each column, amplifies (by operational amplifier) the photoelectric conversion signals of said pixels arranged in the column direction; and outputs said image signals (see Koren, Fig. 1, col. 3, lines 11-13).

6. Claims 2, 11, 16/2 & 16/11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koren et al. (US 6,831,686 B1) and Park (US 2003/0202111 A1) and in further view of Chiu (US 2003/0016294 A1).

Regarding claim 2, as discussed in claim 7 above, the combined teaching of Koren and Park discloses that the color sensitivity correction circuit comprises a first offset and a second offset that are stored in a memory (RAM in Fig. 2 of Koren or register in Fig. 6 of Park) and output to add or subtract from the pixel signals. Koren and Park do not fairly disclose the first offset and second offset being stored in a table.

It is well recognized in the art that offsets for image correction can be stored in table format (i.e., a look-up table) so as to provide a compensation apparatus with less storage space and faster accessing speed as suggested by Chiu in Fig. 2 and paragraphs [0005] & [0022].



Therefore, it would have been obvious to one of ordinary skill in the art to store the first and second offsets of the combined apparatus of Koren and Park in a table so as to provide a compensation apparatus with less storage space and faster accessing speed as suggested by Chiu above.

Regarding claim 11, the limitations of claim 11 are also met by the analysis of claim 2.

Regarding claims 16/2 & 16/11, see the analyses of claims 2 and 16/11 above.

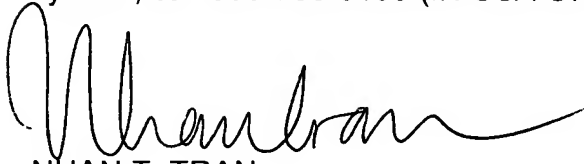
### ***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2622

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

A handwritten signature in black ink, appearing to read 'Nhan Tran', with a stylized, flowing script.

NHAN T. TRAN  
Patent Examiner